

What is claimed is:

- 1     1.     An apparatus comprising:  
2             a power supply node;  
3             a load circuit;  
4             a transistor coupled between the power supply node and the load circuit; and  
5             a control circuit to utilize the transistor as a regulator or a sleep transistor.
- 1     2.     The apparatus of claim 1 wherein the control circuit includes an error  
2             amplifier to influence operation of the transistor.
- 1     3.     The apparatus of claim 1 wherein the control circuit comprises a plurality of  
2             control loops to influence operation of the transistor as a regulator.
- 1     4.     The apparatus of claim 3 wherein the control circuit comprises a first control  
2             loop having an error amplifier.
- 1     5.     The apparatus of claim 4 wherein the control circuit further comprises a  
2             second control loop having a higher bandwidth than the first control loop.
- 1     6.     The apparatus of claim 5 wherein the second control loop is adapted to sense  
2             a voltage between the transistor and the load circuit using a source of a second  
3             transistor.
- 1     7.     The apparatus of claim 1 further comprising:  
2             a second power supply node; and  
3             a second transistor coupled between the load circuit and the second power  
4             supply node;  
5             wherein the control circuit is adapted to utilize the second transistor as a  
6             regulator or a sleep transistor.

1 8. The apparatus of claim 1 wherein the load circuit comprises a memory  
2 circuit.

1 9. The apparatus of claim 1 wherein the load circuit comprises a cache memory  
2 circuit.

1 10. A circuit comprising a sleep transistor coupled between a power supply node  
2 and a load circuit, wherein the sleep transistor is coupled to provide power supply  
3 regulation.

1 11. The circuit of claim 10 further comprising an error amplifier coupled to the  
2 sleep transistor.

1 12. The circuit of claim 11 further comprising a multiplexer coupled between  
2 the error amplifier and the sleep transistor, wherein the multiplexer is adapted to  
3 conditionally turn off the sleep transistor.

1 13. The circuit of claim 10 further comprising a control circuit to conditionally  
2 turn off the sleep transistor.

1 14. The circuit of claim 13 wherein the control circuit comprises a first control  
2 loop including an error amplifier.

1 15. The circuit of claim 14 wherein the control circuit comprises a second  
2 control loop including a sensing transistor coupled to sense a voltage variation using  
3 a source terminal.

1 16. The circuit of claim 15 wherein the control circuit further comprises a bias  
2 transistor coupled between the sensing transistor and a second power supply node.

1 17. The circuit of claim 16 further comprising a voltage divider coupled between  
2 the power supply node and a node formed at a junction between the sensing  
3 transistor and bias transistor, the voltage divider to influence operation of the sleep  
4 transistor.

1 18. The circuit of claim 10 wherein the load circuit comprises a memory circuit.

1 19. The circuit of claim 10 wherein the load circuit comprises a cache memory  
2 circuit.

1 20. The circuit of claim 10 wherein the load circuit is in a first integrated circuit  
2 die, and the sleep transistor is in a second integrated circuit die.

1 21. The circuit of claim 20 wherein the first integrated circuit die is mounted on  
2 top of the second integrated circuit die.

1 22. A method comprising performing power supply regulation using a sleep  
2 transistor.

1 23. The method of claim 22 further comprising turning off the sleep transistor.

1 24. The method of claim 22 further comprising sensing a voltage and  
2 influencing operation of the sleep transistor with an amplifier in a first control loop.

1 25. The method of claim 24 further comprising sensing the voltage and  
2 influencing the operation of the sleep transistor in a second control loop.

1 26. An electronic system comprising:

2           a first integrated circuit including a sleep transistor coupled between a power  
3 supply node and a load circuit, the sleep transistor to provide power supply  
4 regulation; and  
5           a static random access memory device coupled to the first integrated circuit.

1   27.    The electronic system of claim 26 wherein the first integrated circuit further  
2 includes an error amplifier coupled to the sleep transistor.

1   28.    The electronic system of claim 27 wherein the first integrated circuit further  
2 includes a multiplexer coupled between the error amplifier and the sleep transistor,  
3 wherein the multiplexer is adapted to conditionally turn off the sleep transistor.

1   29.    The electronic system of claim 26 wherein the first integrated circuit further  
2 includes a control circuit to conditionally turn off the sleep transistor.

1   30.    The electronic system of claim 29 wherein the control circuit comprises a  
2 first control loop including an error amplifier.